IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (**Currently Amended**) A circuit to calculate the cumulative parity of a binary number sequence, comprising:

an array of functional modules, the modules aligned to form columns and rows within the array, the array configured to receive the binary number sequence at a first column of the modules and to produce the cumulative parity as output at a last column of the modules, each of the modules being one of:

a parity module configured to receive certain input bits from one of the binary number sequence and a previous column and to calculate the parity of the certain input bits; and

a delay module configured to receive other input bits from one of the binary number sequence and a previous column and to delay the other input bits,

wherein

the parity modules form the last column of the modules,

the first column of modules to the second to last column of modules forms an inner array having an equivalent number of rows and columns of modules, and

within the inner array of modules the parity modules form a diagonal of the inner array from a first row to a last row and the delay modules are the remaining modules within the inner array.

2. (Original) The circuit of claim 1, wherein calculations within the array proceed from the first column to the last column and the array includes one more column than row.

3-4. (Canceled)

5. (**Currently Amended**) The circuit of ~~claim 4~~ claim 1, wherein each parity module comprises:

n parallel inputs;

an initial parity input at which to receive an initial parity bit; and

n parallel outputs, wherein the ith bit of the n parallel outputs is the parity of the first i bits of the n parallel inputs and the initial parity input.

6. (Original) The circuit of claim 5, wherein after one clock cycle following the arrival of certain input bits at the n parallel inputs, resultant output bits are provided from the n parallel outputs.

7. (**Currently Amended**) The circuit of claim 1, wherein any delay modules within the same row of the array[[,]] have the same number of inputs and outputs.

8. (Original) The circuit of claim 1, wherein within a given row of the array, the number of parallel inputs and outputs of any parity module is equal to the number of inputs and outputs of any delay module.

9. (Original) The circuit of claim 5, wherein the last parallel output of each parity module that forms a diagonal within the inner array of the array, except for the parity module in the last row of the inner array, is connected to the initial parity input of the parity module in the next column and the next row.

10. (Original) The circuit of claim 5, wherein the last parallel output of the parity module in the last row and the last column is connected to the initial parity input of each parity module in the last column.

11. (Original) The circuit of claim 5, wherein the initial parity input of the parity module in the first row and the first column is connected to logic zero.

12. (Original) The circuit of claim 5, wherein each delay module comprises:

n parallel inputs; and

n parallel outputs; wherein output bits on the n parallel outputs are equivalent to other input bits received at the n parallel inputs, delayed for one clock cycle.

13. (Original) The circuit of claim 12, wherein the n parallel outputs of a given module of the array in a given row and column of the array, except for the last column, are connected to the n parallel inputs of the module in the same row and the next column of the array.

14. (Original) The circuit of claim 1, wherein a number of inputs of the party module exceed the a number of outputs of the parity module by one, wherein output bits are provided from the outputs of the parity module, and wherein the first output provides a first output bit that is the parity of the certain input bits received at the first two inputs, the second output provides a second output bit that is the parity of the certain input bits received at the first three inputs, and the ith output provides an ith output bit that is the parity of the certain input bits received at the first i +1 outputs.

15. (Original) The circuit of claim 1, wherein a first number of other input bits received by a delay module in one row of the array is not equivalent to a second number of other input bits received by a delay module in another row of the array.

16. (Original) The circuit of claim 1, wherein a first number of certain input bits received by a parity module in one row of the array is not equivalent to a second number of certain input bits received by a parity module in another row of the array.

17. (Original) The circuit of claim 1, further comprising:

at least one circuit element to align the timing and the delay of logic gates within the circuit and the array.

18. (Original) The circuit of claim 1, wherein each delay module comprises at least one D-type flip flop.

19. (Original) The circuit of claim 1, wherein each delay module comprises a bank of D-type flip-flops.

20. (Original) The circuit of claim 1, wherein each delay module comprises a component having a triggered delay for one clock cycle.

21. (Original) The circuit of claim 1, wherein each parity module comprises at least one D-type flip-flop.

22. (Original) The circuit of claim 1, wherein, each parity module comprises at least one XOR gate and at least one D-type flip-flop.

23. (Original) The circuit of claim 1, wherein each parity module comprises a ladder of XOR gates and a bank of D-type flip-flops.

24. (Original) The circuit of claim 1, wherein each parity module comprises a ladder of XOR gates, a bank of XOR gates, and a bank of D-type flip-flops.

25. (Original) The circuit of claim 1, wherein the circuit is used as the differential precoder before a time-division multiplexer for a duobinary transmitter in an optical communication system.

26. (Original) The circuit of claim 1, wherein the circuit is used as the differential precoder for duobinary transmission, the differential precoder operating in parallel and having at least two parallel inputs.

27. (Original) A circuit to calculate the cumulative parity of a binary number sequence, comprising:

an array of delay elements, the delay elements aligned to form M + 1 columns and M rows within the array, where M represents a number of parallel input bit values, and wherein the array is configured to receive the binary number sequence at the first column of the delay elements and to produce the cumulative parity as output at the (M+1)th column of the delay elements, the array comprising:

diagonal delay elements forming a diagonal of an M column by M row inner array of the array, from the first row and the first column to the Mth row and the Mth column of the array;

non-diagonal delay elements, wherein the non-diagonal delay elements are the remaining delay elements within the inner array; and

the (M+1)th column delay elements;

diagonal gate elements located from the second row through the Mth rows of the array to calculate parity information, the diagonal gate elements each having a diagonal gate output connected to a diagonal delay input of the corresponding diagonal delay element in the same row and the next column of the array, a first diagonal gate input connected to a diagonal delay output of the corresponding diagonal delay element in the prior row and the previous column of the array, and a second diagonal gate input connected to a non-diagonal delay output of the corresponding non-diagonal delay element in the same row and the previous column of the array; and

column gate elements located from the first row to the Mth row of the array and between the Mth column and the (M+1)th column of the array, the column gate elements each having a column gate output connected to a column delay input of the corresponding (M+1)th column delay element in the same row of the array, the column gate elements used to pass the parity information from the diagonal and non-diagonal outputs of respective diagonal and non-diagonal delay elements in prior columns of the array to the (M+1)th column delay elements.

28. (Original) The circuit of claim 27, wherein the diagonal and column gate element each comprise an XOR gate.

29. (Original) The circuit of claim 27, wherein for any of the diagonal delay elements in the first through the (M-1)th columns, the respective diagonal delay output is connected to

the non-diagonal delay output of the corresponding non-diagonal delay element in the same row and the next column of the array.

30. (Original) The circuit of claim 27, wherein the column gate elements each have a column gate input connected to a column delay output of the (M+1)th column delay element in the Mth row of the array.

31. (Original) The circuit of claim 30, wherein the column gate elements from the first row to the (M-1)th row of the array each have a second column gate input connected to the non-diagonal delay output of the corresponding non-diagonal delay element in the Mth column of the array.

32. (Original) The circuit of claim 30, wherein the column gate element in the Mth row of the array has a second column gate input connected to the diagonal delay output of the diagonal delay element in the Mth row of the array.

33. (Original) A method of using an array of M(M+1) modules to calculate the cumulative parity of a binary number sequence, the array comprising M rows of M+1 modules and M+1 columns of M modules, the method comprising:

within a first clock cycle T:

calculating the cumulative parity of a first input group of n input bit values and a first initial parity input value at the first row first column module;

delaying a second input group of n input bit values at the second row first column module; and

delaying an Mth input group of n input bit values at the Mth row first column module;

within a second clock cycle 2T:

delaying the cumulative parity of the first input group at the first row second column module;

calculating the cumulative parity of the second input group and a second initial parity input bit value at the second row second column module; and

delaying the Mth input group at the Mth row second column module;

within an Mth clock cycle MT:

delaying the cumulative parity of the first input group at the first row Mth column module;

delaying the cumulative parity of the second input group at the second row Mth column module; and

calculating the cumulative parity of the Mth input group and an Mth initial parity input bit value at the Mth row Mth column module; and

within an (M+1)th clock cycle (M+1)T:

calculating a first output group of n output bit values at the first row (M+1)th column module;

calculating a second output group of n output bit values at the second row (M+1)th column module; and

calculating an Mth output group of n output bit values at the Mth row (M+1)th column module.

34. (Original) The method of claim 33, wherein the first row first column module, the second row second column module, and the Mth row Mth column module are parity modules.

35. (Original) The method of claim 33, wherein all modules in the (M+1)th column of the array are parity modules.

36. (Original) The method of claim 33, wherein the second row first column module, the Mth row first column module, the first row second column module, the Mth row second column module, the first row Mth column module, and the second row Mth column module are delay modules.

37. (Original) The method of claim 33, wherein the nth output bit value of the first output group is the cumulative parity of n output bit values of the first row Mth column module and of an (M+1)th initial parity input bit value.

38. (Original) The method of claim 37, wherein the nth output bit value of the second output group is the cumulative parity of n output bit values of the second row Mth column module and of the (M+1)th initial parity input bit value.

39. (Original) The method of claim 38, wherein the nth output bit value of the Mth output group is the cumulative parity of n output bit values of the Mth row Mth column module and of the (M+1)th initial parity input bit value.

40. (Original) The method of claim 39, wherein the (M+1)th initial parity input bit value is the nth output bit value of the Mth output group, delayed by one clock cycle T.

41. (Original) A method of calculating the cumulative parity of a binary number sequence using an array of parity and delay modules, the array comprising M rows of M+1 modules and M+1 columns of M modules, the method comprising:

receiving the binary number sequence at a series of inputs at the first column of the array;

calculating parity information using parity modules of the array;

passing parity information through the array, column by column, from the first column to the (M+1)th column;

aligning the timing of the parity information using delay modules of the array; and

providing the cumulative parity of the binary number sequence at a series of outputs at the (M+1)th column of the array.

42. (Original) A system to calculate the cumulative parity of a binary number sequence using an array of modules, the array comprising M rows of M+1 modules and M+1 columns of M modules, the method comprising:

means for receiving the binary number sequence at a series of inputs at the first column of the array;

means for calculating parity information;

means for passing parity information through the array, column by column, from the first column to the (M+1)th column;

means for aligning the timing of the parity information; and

means for providing the cumulative parity of the binary number sequence at a series of outputs at the (M+1)th column of the array.